

Claim Amendments:

Please amend the claims as indicated:

Claims 1-18 (Withdrawn)

19. (Currently Amended) An electronic package~~A multi-chip module~~, comprising:
a first semiconductor device capable of enabling functionality associated with a first circuit segment of an integrated circuit design and ~~including an array~~including a set of first device interconnect pads;
a second semiconductor device capable of enabling functionality associated with a second circuit segment of the integrated circuit design and ~~including an array~~including a set of second device interconnect pads; and
a plurality of device interconnect members, each one of said device interconnect members being electrically connected directly between one of said first device interconnect pads and a corresponding one of said second device interconnect pads.
20. (Currently Amended) The electronic package~~multi-chip module~~ of claim 19 wherein:
the first semiconductor device~~includes~~ is capable of enabling functionality associated with a first functional block of the integrated circuit design; and
the second semiconductor device~~device~~ is capable of enabling functionality associated with a second functional block of the integrated circuit design.
21. (Currently Amended) The electronic package~~multi-chip module~~ of claim 19 wherein:
the first semiconductor device is a DRAM device; and
the second semiconductor device is a logic device.
22. (Currently Amended) The electronic package~~multi-chip module~~ of claim 19 wherein:

PATENT

the first semiconductor device is made from a first type of semiconductor substrate; and
the second semiconductor device is made from a second type of semiconductor substrate.

23. (Currently Amended) The electronic package~~multi-chip module~~ of claim 19
wherein each one of said device interconnect members is a solder-type interconnect member.

24. (Currently Amended) The electronic package~~multi-chip module~~ of claim 23
wherein the solder-type interconnect member is a solder bump.

25. (Currently Amended) The electronic package~~multi-chip module~~ of claim 23
wherein the solder-type interconnect member is a solder ball.

26. (Currently Amended) The electronic package of claim 19 wherein the electronic
package is a multichip module and the plurality of device interconnect members includes solder-
type interconnect members.~~A multi-chip module, comprising:~~

~~a first semiconductor device capable of enabling functionality associated with a first
functional block of an integrated circuit design and including an array of first
device interconnect members;~~

~~a second semiconductor device capable of enabling functionality associated with a
second functional block of the integrated circuit design and including an array of
second device interconnect members; and~~

~~a plurality of solder-type interconnect members, each one of said solder-type interconnect
members being electrically connected directly between one of said first device
interconnect members and a corresponding one of said second device interconnect
members.~~

27. (Currently Amended) The electronic package~~multi-chip module~~ of claim 26
wherein:

the first semiconductor device is a DRAM device; and
the second semiconductor device is a logic device.

PATENT

28. (Currently Amended) The electronic package~~multi-chip module~~ of claim 26 wherein:

the first semiconductor device is made from a first type of semiconductor substrate; and
the second semiconductor device is made from a second type of semiconductor substrate.

29. (Currently Amended) The electronic package~~multi-chip module~~ of claim 26 wherein the solder-type interconnect member is a solder bump.

30. (Currently Amended) The electronic package~~multi-chip module~~ of claim 26 wherein the solder-type interconnect member is a solder ball.

31. (Currently Amended) ~~An electronic package;~~ The electronic package of claim 19,
further comprising:

an interposer circuit including a dielectric substrate and an array of routing elements
attached to the dielectric substrate; and

~~a first semiconductor device capable of enabling functionality associated with a first
circuit segment of an integrated circuit design and including an array of first
device interconnect pads;~~

~~a second the second semiconductor device capable of enabling functionality associated
with a second circuit segment of the integrated circuit design, including an array
of second device interconnect pads and including~~ further comprising a set of
package-level interconnect pads; and

~~a plurality of device interconnect members, each one of said device interconnect
members being electrically connected directly between one of the said first device
interconnect pads and a corresponding one of said second device interconnect
pads; and~~

a plurality of package-level interconnect members, each one of said package-level
interconnect members being electrically connected between one of the said
package-level interconnect pads of the second semiconductor device and a
corresponding one of said routing elements of the interposer circuit.

32. (Original) The electronic package of claim 31 wherein:

PATENT

the first semiconductor device includes is capable of enabling functionality associated with a first functional block of the integrated circuit design; and
the second semiconductor device is capable of enabling functionality associated with a second functional block of the integrated circuit design.

33. (Original) The electronic package of claim 31 wherein:
the first semiconductor device is a DRAM device; and
the second semiconductor device is a logic device.

34. (Original) The electronic package of claim 31 wherein:
the first semiconductor device is made from a first type of semiconductor substrate; and
the second semiconductor device is made from a second type of semiconductor substrate.

35. (Original) The electronic package of claim 31 wherein each one of said device interconnect members is a solder-type interconnect member.

36. (Original) The electronic package of claim 35 wherein the solder-type interconnect member is a solder bump.

37. (Original) The electronic package of claim 35 wherein the solder-type interconnect member is a solderball.

38. (Original) The electronic package of claim 31 wherein:
the interposer circuit is a flip-chip interposer circuit; and
each one of said package-level interconnect members is a solder-type interconnect member.

39. (Original) The electronic package of claim 31 wherein:
the interposer circuit is a wire-bond interposer circuit; and
each one of said package-level interconnect members is a conductive wire.

40. (Canceled)

PATENT

41. (Currently Amended) The electronic package of ~~claim 35~~claim 40 wherein:
the first semiconductor device is a DRAM device; and
the second semiconductor device is a logic device.
42. (Currently Amended) The electronic package of ~~claim 35~~claim 40 wherein:
the first semiconductor device is made from a first type of semiconductor substrate; and
the second semiconductor device is made from a second type of semiconductor substrate.
43. (Currently Amended) The electronic package of ~~claim 35~~claim 40 wherein the
solder-type interconnect member is a solder bump.
44. (Currently Amended) The electronic package of ~~claim 40~~claim 35 wherein the
solder-type interconnect member is a solder ball.
45. (Currently Amended) The electronic package of ~~claim 40~~claim 35 wherein:
the interposer circuit is a flip-chip interposer circuit; and
each one of said package-level interconnect members is a solder-type interconnect
member.
46. (Currently Amended) The electronic package of ~~claim 40~~claim 35 wherein:
the interposer circuit is a wire-bond interposer circuit; and
each one of said package-level interconnect members is a conductive wire.